REMARKS/ARGUMENT

1) Claims 11-14 are rejected under 35 U.S.C. 101 as being directed to non-statutory subject matter. Applicants respectfully traverse this rejection, as set forth below.

Independent Claim 11 requires and positively recites, a method for performing saturated arithmetic **in an electronic apparatus**, comprising: **"receiving** an unsaturated output **from a processing unit in said electronic apparatus", "processing** the unsaturated output **to produce a saturated output upon occurrence of an overflow or underflow condition"** and **"selecting between the saturated output and unsaturated output based on the state of a programmable saturation control bit".**

Applicants respectfully point out that the above high-lighted elements/steps surely qualify as "transforming" an article or physical object to a different states or thing. At the very minimum, the invention of Claim 11 otherwise produces a useful, concrete and tangible result. Accordingly, the 35 U.S.C. 101 rejection is improper and must be withdrawn.

Claims 12-14 depend from Claim 11 and similarly comply with 35 U.S.C. 101. Accordingly, the 35 U.S.C. 101 rejection of these claims is similarly improper and must be withdrawn.

2) Claims 1-17 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Perets et al. (U.S. 6,535,900). Applicants respectfully traverse this rejection, as set forth below.

In order that the rejection of Claims 1-17 be sustainable, it is fundamental that "each and every element as set forth in the claim be found, either expressly or inherently described, in a single prior art reference." *Verdegall Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See also, *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), where the court states, "The identical invention must be shown in as complete detail as is contained in the ... claim".

Furthermore, "all words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Independent Claim 1, as amended, requires and positively recites, a processor, comprising: "a programmable saturation control bit", "a processing unit that produces an unsaturated output", "a saturation unit coupled to the processing unit **and that produces an output that is saturated upon the occurrence of an underflow or overflow condition**" and "a selection unit that **receives the outputs from the processing and saturation units and selects one of the two outputs as an output from the selection unit** based on the state of the saturation control bit".

Independent Claim 11 requires and positively recites, a method for performing saturated arithmetic in an electronic apparatus, comprising: "receiving an unsaturated output from a processing unit in said electronic apparatus", "processing the unsaturated output to produce a saturated output **upon occurrence of an overflow or underflow condition**" and "**selecting between the saturated output and unsaturated output** based on the state of a programmable saturation control bit".

Independent Claim 15 requires and positively recites, a processor, comprising: "a means for performing an unsaturated operation to produce an unsaturated value", "a means for saturating the unsaturated value to produce a saturated value" and "a means

for dynamically selecting between the unsaturated value and the saturated value based upon a mode bit that indicates whether saturated or unsaturated operations are to be performed".

In contrast, Perets discloses a saturation (SAT) unit 22 (col. 3, lines 25, 38-41) – NOT unit 24 as determined by Examiner. Indication generator 24 (SDET) determines whether the value being written to accumulator 14 is overflowed and whether the overflow is positive or negative. This indication is input to SAT unit 22, allowing SAT unit 22 to generate the correct saturated value in the feedback loop to CU 12 (col. 3, lines 43-48). Thus, Perets' saturation (SAT) unit 22 produces a saturation result in response to a positive indication of a saturation result from indication generator 24 (SDET) – NOT "upon the occurrence of an underflow or overflow condition", as taught by the present invention. As such, Perets fails to teach or suggest, "a saturation unit coupled to the processing unit and that produces an output that is saturated upon the occurrence of an underflow or overflow condition", as required by Claim 1, OR "processing the unsaturated output to produce a saturated output upon occurrence of an overflow or underflow condition", as required by Claim 11.

In the present invention, saturation unit 108 always produces an output that is saturated upon the occurrence of an underflow or overflow condition. It is then up to multiplexer 106 to select between the saturated output from saturation unit 108 or the unsaturated output from ALU 104.

Moreover, Perets SDET 24 does not select "between" a saturated signal from CU 12 and SAT unit 22 – if an overflow determination is made, SDET 24 gives a command to SAT unit 22 to saturate the unsaturated signal from CU 12, which is then passed back to CU 12. As such, Perets fails to further teach or suggest, "a selection unit that receives the outputs from the processing and saturation units and selects one of the two outputs as an output from the selection unit based on the state of the

saturation control bit", as required by Claim 1, OR "selecting between the saturated output and unsaturated output based on the state of a programmable saturation control bit", as required by Claim 11, OR "a means for dynamically selecting between the unsaturated value and the saturated value based upon a mode bit that indicates whether saturated or unsaturated operations are to be performed", as required by Claim 15. Accordingly, the 35 U.S.C. 102(e) rejection of Claims 1, 13 and 19 is overcome.

Claims 2-10, 12-14, 16 and 17 stand allowable as depending directly, or indirectly, respectively from allowable Claims 1, 11 and 15. Claim 2 depends from Claim 1 and stands allowable for the same reasons set forth above in support of the allowability of Claim 1.

Claim 2 further defines the processor of claim 1 wherein the processing unit comprises an arithmetic logic unit. Claim 2 depends from Claim 1 and stands allowable for the same reasons set forth above in support of the allowability of Claim 1.

Claim 3 further defines the processor of claim 1 wherein the processing unit comprises a multiply and accumulate unit. Claim 3 depends from Claim 1 and stands allowable for the same reasons set forth above in support of the allowability of Claim 1.

Claim 4 further defines the processor of claim 1 wherein the selection unit comprises a multiplexer. Claim 4 depends from Claim 1 and stands allowable for the same reasons set forth above in support of the allowability of Claim 1.

Claim 5 further defines the processor of claim 1 wherein the saturation unit forces the saturated output to be a maximum value if an overflow occurs in the processing unit. Claim 5 depends from Claim 1 and stands allowable for the same reasons set forth above in support of the allowability of Claim 1.

Claim 6 further defines the processor of claim 1 wherein the saturation unit forces the saturated output to be a minimum value if an underflow occurs in the processing unit. Claim 6 depends from Claim 1 and stands allowable for the same reasons set forth above in support of the allowability of Claim 1.

Claim 7 further defines the processor of claim 1 wherein the saturation control bit is programmed through an application programming interface. Claim 7 depends from Claim 1 and stands allowable for the same reasons set forth above in support of the allowability of Claim 1.

Claim 8 further defines the processor of claim 1 wherein the saturation control bit is programmed through an assembly language macro that is instantiated in high-level code. Claim 8 depends from Claim 1 and stands allowable for the same reasons set forth above in support of the allowability of Claim 1.

Claim 9 further defines the processor of claim 1 wherein the saturation control bit is programmed through a compiler through a specific pragma. Claim 9 depends from Claim 1 and stands allowable for the same reasons set forth above in support of the allowability of Claim 1.

Claim 10 further defines the processor of claim 1 wherein the saturation control remains set for multiple instructions. Claim 10 depends from Claim 1 and stands allowable for the same reasons set forth above in support of the allowability of Claim 1.

Claim 12 further defines the method of claim 11 wherein the saturation control bit is programmed through an application programming interface to cause either saturated or non-saturated operations to be performed. Claim 12 depends from Claim 10 and stands allowable for the same reasons set forth above in support of the allowability of Claim 10.

Claim 13 further defines the method of claim 11 wherein processing the unsaturated output comprises forcing the saturated output to be a maximum value if an overflow occurs in the processing unit. Claim 13 depends from Claim 11 and stands allowable for the same reasons set forth above in support of the allowability of Claim 11.

Claim 14 further defines the method of claim 11 wherein processing the unsaturated output comprises forcing the saturated output to be a minimum value if an underflow occurs in the processing unit. Claim 14 depends from Claim 11 and stands allowable for the same reasons set forth above in support of the allowability of Claim 11.

Claim 16 further defines the processor of claim 15 further comprising a means for setting the mode bit. Claim 16 depends from Claim 15 and stands allowable for the same reasons set forth above in support of the allowability of Claim 15.

Claim 17 further defines the processor of claim 15 wherein the mode bit remains set for the execution of multiple instructions. Claim 17 depends from Claim 15 and stands allowable for the same reasons set forth above in support of the allowability of Claim 15.

3) Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okayama (Applicant cited EP 0 657 804). Applicants respectfully traverse this rejection, as set forth below.

Independent Claim 1, as amended, requires and positively recites, a processor, comprising: "a programmable saturation control bit", "a processing unit that produces

an unsaturated output", "a saturation unit coupled to the processing unit **and that produces an output that is saturated upon the occurrence of an underflow or overflow condition**" and "a selection unit that receives **the outputs from the processing and saturation units and selects one of the two outputs as an output from the selection unit** based on the state of the saturation control bit".

Independent Claim 11 requires and positively recites, a method for performing saturated arithmetic in an electronic apparatus, comprising: "receiving an unsaturated output from a processing unit in said electronic apparatus", "processing the unsaturated output to produce a saturated output **upon occurrence of an overflow or underflow condition**" and "**selecting between the saturated output and unsaturated output based on the state of a programmable saturation control bit**".

Independent Claim 15 requires and positively recites, a processor, comprising: "a means for performing an unsaturated operation to produce an unsaturated value", "a means for saturating the unsaturated value to produce a saturated value" and "a means for dynamically selecting between the unsaturated value and the saturated value based upon a mode bit that indicates whether saturated or unsaturated operations are to be performed".

In contrast, Okayama discloses: an ALU (1); an instruction decoder (2) that outputs the arithmetic operation command 35 to the saturation detecting circuit 3 and the flag generator 4 (page 4, lines 19-20); a saturation detecting circuit (3) that outputs to the flag generator 4 a status signal indicating that the saturation processing has been performed and selectively activates selection signals 32, 33 and 34 for selecting the result of arithmetic operation. None of: flag generator 4; saturation detecting circuit 3; or instruction decoder 2 produce an output that is saturated. As such, Okayama fails to teach or suggest, "a saturation unit coupled to the processing unit **and that produces an output that is saturated upon the occurrence of an underflow or overflow**

condition", as required by Claim 1, OR "processing the unsaturated output to produce a saturated output upon occurrence of an overflow or underflow condition", as required by Claim 11.

In the present invention, saturation unit 108 always produces an output that is saturated upon the occurrence of an underflow or overflow condition. It is then up to multiplexer 106 to select between the saturated output from saturation unit 108 or the unsaturated output from ALU 104.

Moreover, there is no teaching in Okayama of a selection unit that receives outputs from both the processing AND saturation units and thereafter selects one of the two outputs. As such, Okayam fails to further teach or suggest, "a selection unit that receives the outputs from the processing and saturation units and selects one of the two outputs as an output from the selection unit based on the state of the saturation control bit", as required by Claim 1, OR "selecting between the saturated output and unsaturated output based on the state of a programmable saturation control bit", as required by Claim 11, OR "a means for dynamically selecting between the unsaturated value and the saturated value based upon a mode bit that indicates whether saturated or unsaturated operations are to be performed", as required by Claim 15. Accordingly, the 35 U.S.C. 103(a) rejection of Claims 1, 13 and 19 is overcome.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. (MPEP § 2143).

Moreover, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." *In re Kotzab,* 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also *In re Lee,* 277 F.3d 1338, 1342-44, 61 USPQ2d 1430, 1433-34 (Fed. Cir. 2002) (discussing the importance of relying on objective evidence and making specific factual findings with respect to the motivation to combine references); ***In re Fine,*** 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); ***In re Jones,*** **958 F.2d 347, 21** USPQ2d 1941 (Fed. Cir. 1992).

Applicants further point out that a statement that modifications of the prior art to meet the claimed invention would have been "well within the ordinary skill of the art at the time the claimed invention was made" because the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a *prima facie* case of obviousness without some objective reason to combine the teachings of the references. *Ex parte Levengood,* 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993). See also *In re Kotzab,* 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1318 (Fed. Cir. 2000) (Court reversed obviousness rejection involving technologically simple concept because there was no finding as to the principle or specific understanding within the knowledge of a skilled artisan that would have motivated the skilled artisan to make the claimed invention); *Al-Site Corp. v. VSI Int'l Inc.*, 174 F.3d 1308, 50 USPQ2d 1161 (Fed. Cir. 1999) (The level of skill in the art cannot be relied upon to provide the suggestion to combine references).

Claims 2-10, 12-14, 16 and 17 stand allowable as depending directly, or indirectly, respectively from allowable Claims 1, 11 and 15. Claim 2 depends from

Claim 1 and stands allowable for the same reasons set forth above in support of the allowability of Claim 1.

Claim 2 further defines the processor of claim 1 wherein the processing unit comprises an arithmetic logic unit. Claim 2 depends from Claim 1 and stands allowable for the same reasons set forth above in support of the allowability of Claim 1.

Claim 3 further defines the processor of claim 1 wherein the processing unit comprises a multiply and accumulate unit. Claim 3 depends from Claim 1 and stands allowable for the same reasons set forth above in support of the allowability of Claim 1.

Claim 4 further defines the processor of claim 1 wherein the selection unit comprises a multiplexer. Claim 4 depends from Claim 1 and stands allowable for the same reasons set forth above in support of the allowability of Claim 1.

Claim 5 further defines the processor of claim 1 wherein the saturation unit forces the saturated output to be a maximum value if an overflow occurs in the processing unit. Claim 5 depends from Claim 1 and stands allowable for the same reasons set forth above in support of the allowability of Claim 1.

Claim 6 further defines the processor of claim 1 wherein the saturation unit forces the saturated output to be a minimum value if an underflow occurs in the processing unit. Claim 6 depends from Claim 1 and stands allowable for the same reasons set forth above in support of the allowability of Claim 1.

Claim 7 further defines the processor of claim 1 wherein the saturation control bit is programmed through an application programming interface. Claim 7 depends from Claim 1 and stands allowable for the same reasons set forth above in support of the allowability of Claim 1.

Claim 8 further defines the processor of claim 1 wherein the saturation control bit is programmed through an assembly language macro that is instantiated in high-level code. Claim 8 depends from Claim 1 and stands allowable for the same reasons set forth above in support of the allowability of Claim 1.

Claim 9 further defines the processor of claim 1 wherein the saturation control bit is programmed through a compiler through a specific pragma. Claim 9 depends from Claim 1 and stands allowable for the same reasons set forth above in support of the allowability of Claim 1.

Claim 10 further defines the processor of claim 1 wherein the saturation control remains set for multiple instructions. Claim 10 depends from Claim 1 and stands allowable for the same reasons set forth above in support of the allowability of Claim 1.

Claim 12 further defines the method of claim 11 wherein the saturation control bit is programmed through an application programming interface to cause either saturated or non-saturated operations to be performed. Claim 12 depends from Claim 10 and stands allowable for the same reasons set forth above in support of the allowability of Claim 10.

Claim 13 further defines the method of claim 11 wherein processing the unsaturated output comprises forcing the saturated output to be a maximum value if an overflow occurs in the processing unit. Claim 13 depends from Claim 11 and stands allowable for the same reasons set forth above in support of the allowability of Claim 11.

Claim 14 further defines the method of claim 11 wherein processing the unsaturated output comprises forcing the saturated output to be a minimum value if an

underflow occurs in the processing unit. Claim 14 depends from Claim 11 and stands allowable for the same reasons set forth above in support of the allowability of Claim 11.

Claim 16 further defines the processor of claim 15 further comprising a means for setting the mode bit. Claim 16 depends from Claim 15 and stands allowable for the same reasons set forth above in support of the allowability of Claim 15.

Claim 17 further defines the processor of claim 15 wherein the mode bit remains set for the execution of multiple instructions. Claim 17 depends from Claim 15 and stands allowable for the same reasons set forth above in support of the allowability of Claim 15.

Claims 1-17 stand allowable. Applicants respectfully request withdrawal of the remaining rejections and allowance of the application at the earliest possible date.

Respectfully submitted,

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